Comment on "Reducing error rates in straintronic multiferroic nanomagnetic logic by pulse shaping" [Nanotechnology 26, 245202 (2015)]

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In Ref. 1, the authors proposed to reduce error probability of switching in a system of *two* dipole-coupled magnetostrictive nanomagnets in strain-mediated multiferroic heterostructures using voltage (stress) pulse shaping. The authors conclude that high success probability of switching *cannot* be achieved at high switching speed (∼1 ns), and therefore their proposed system is only applicable for niche applications. However, such conclusion lacked the critical understandings behind such high error probability for general-purpose logic applications. Fortunately, such analysis and a possible solution along the line of the analysis is present in literature [2] using Bennett clocking [3] for logic design, on which Ref. 1 (and arXiv version Ref. 4) has made some *incorrect* statements. Earlier, a subset of the authors of Ref. 1 also published a paper [5] on a *four* magnet system using the Bennett clocking mechanism, where the authors also came up with a similar conclusion of high error probability and the demise of multiferroic nanomagnetic logic, however, without relevant analysis similar to the case as in the Ref. 1.

First, the Fig. 1 in Ref. 1 shows the directions of unit vectors in standard Cartesian coordinate system (x-y-z) incorrectly (one correct option is to interchange x and y), and also the demagnetization factors in the Equations (7), (8), and (9) are incorrect. This may have produced incorrect results in the paper [1]. In any case, a correct coordinate system will be utilized in this Comment as shown in Fig. 1(a).

The Fig. 2(c) in Ref. 1 concerns about the *in-plane* potential landscape of the nanomagnets to analyze the error probability, however, the critical analysis in Ref. 2 has shown that it is the *out-of-plane* motion that is responsible for high error probability and a solution along the line of such critical analysis was presented. The intriguing dynamics of a complete 180° switching for a single magnetostrictive nanomagnet has been studied elaborately in Refs. 6, 7. The torque due to stress acts in the out-of-plane ($\hat{\mathbf{e}}_\phi$ in Fig. 1) direction as

$$\mathbf{T_{E,stress}} = -\hat{\mathbf{e}}_\mathbf{r} \times \nabla E_{stress} = -(3/2)\,\lambda_s \sigma sin(2\theta)\,\hat{\mathbf{e}}_\phi, \tag{1}$$

where $E_{stress} = -(3/2)\,\lambda_s \sigma cos^2\theta$ is the potential energy due to stress per unit volume, $(3/2)\lambda_s$ is the magnetostrictive coefficient, and σ is the stress. If such out-of-plane

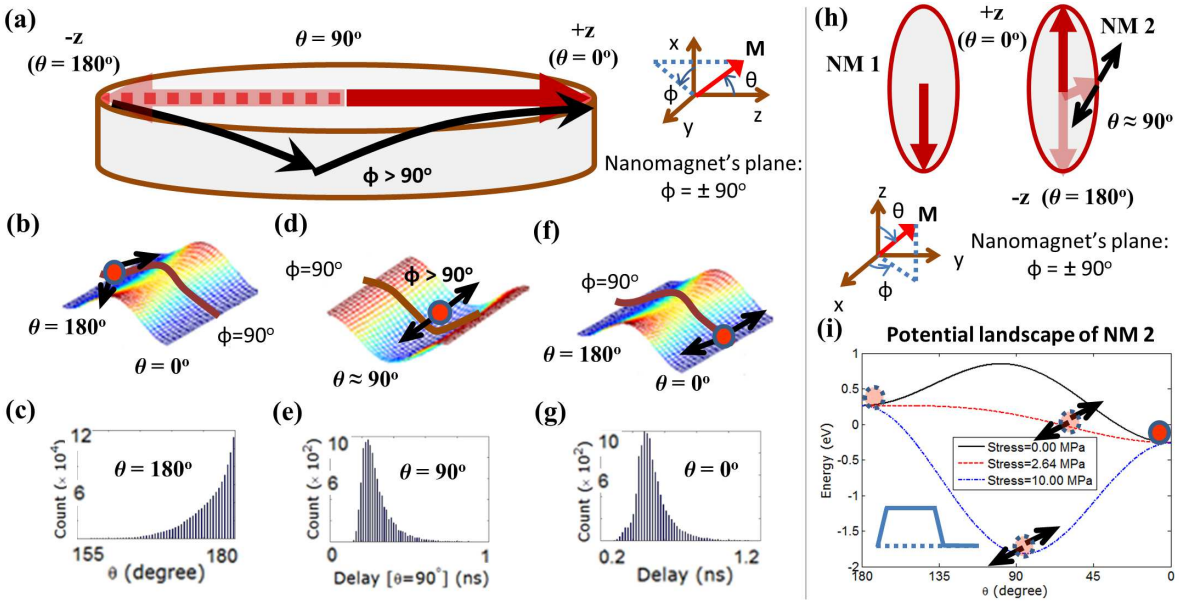

Figure 1. (a) The out-of-plane excursion of magnetization and axis assignment. (b), (c) Three-dimensional potential landscape of the nanomagnet and the distribution of magnetization in the presence of room-temperature (300 K) thermal fluctuations. The solid line depicts the *in-plane* potential landscape. (d), (e) The same as (b), (c) when magnetization reaches $\theta = 90°$. (f), (g) The same as (b), (c) when magnetization reaches $\theta \simeq 180°$. [parts (c), (e), and (g) are taken from Refs. 6, 7.] (h) Two-magnet system depicting that the second nanomagnet (NM 2) deflects out-of-plane when reaching $\theta \simeq 90°$ upon application of stress. (i) Potential landscapes of NM 2 with stress as a parameter depicting the successful traversal of magnetization from $\theta \simeq 180°$ to $\theta \simeq 0°$ upon application and withdrawal of stress.

motion is *not* considered, the complete 180° motion cannot be possible [6, 7]. Also such switching is confirmed by others [8–10]. Such out-of-plane motion also increases the switching speed to the order of GHz [6, 7].

Ref. 11 *incorrectly* assumed only *in-plane* motion of magnetization for logic design using Bennett clocking, and the switching delay of magnetization according to Ref. 11 is ∼1000 ns, and that is clearly *untenable* for building general purpose nanoelectronics [12, 13]. Fortunately, the analysis in Ref. 11 is incorrect and it was corrected by Roy for memory design [6, 7, 14–17] and also for logic design [14, 18, 19]. Similarly, in the presence of thermal fluctuations, the critical analysis due to *out-of-plane* excursion of magnetization is missing in Refs. 1,4,5 for logic design purposes with wrong conclusions of high switching delay and high error probability; correct analysis has been performed by Roy in Ref. 2. Such out-of-plane motion also plays important role in determining the pertinent energy dissipation [20–22].

Ref. 1 has made the following *incorrect* statements on Ref. 2, as explained below.

(1) Ref. 1 states while referring Ref. 2 that "it examined switching errors in straintronic memory (not logic)". This is preposterous since Fig. 1(b) in Ref. 2 clearly shows the logic design using Bennett clocking for four-nanomagnet system and the underlying

equations are also derived and provided. Actually, Ref. 1 analyzed only *two* nanomagnet system, therefore, the system in Ref. 1 is *incomplete* to be termed as logic design.

(2) Ref. 1 states while referring Ref. 2 that "A feedback circuit will determine when the magnetization has rotated by 90° ... at that juncture." This has been already stated and explained in literature [6, 7] and Ref. 1 stated it *quite inaccurately*. Fig. 1(a) shows that magnetization gets deflected out-of-plane due to the torque exerted on it [see Equation (1)]. The three-dimensional potential landscapes are also shown in the Figs. 1(b), (d), (f), depicting the out-of-plane motion of magnetization. Due to thermal fluctuations, the initial angle distribution of magnetization [Fig. 1(c)] and the time it takes to reach $\theta = 90°$ is a *wide* distribution [Fig. 1(e)]. Stress needs to be withdrawn when magnetization reaches *around* $\theta = 90°$ so that magnetization traverses towards $\theta \simeq 0°$ [switching delay distribution is shown in Fig. 1(g)], and does not backtrack towards $\theta \simeq 180°$, causing switching failure [6,7]. This is purely dynamical phenomenon [6,7] contrary to stead-state analysis. Therefore, a sensing element is required to detect when magnetization reaches around $\theta = 90°$ [6, 7]. The sensing element can be a spin valve or magnetic tunnel junction (MTJ), which is required to read the magnetization state [6, 7, 23]. We can get calibrated on the magnetoresistance of the spin valve or MTJ when $\theta = 90°$ and comparing this known signal with the sensed signal of the MTJ, the stress can be ramped down [6, 7]. According to the study presented in Refs. 6, 7, note that there is tolerance around $\theta = 90°$, i.e., stress does not need to be withdrawn precisely *at the juncture* $\theta = 90°$ (this was also *incorrectly* stated in Refs. 21, 24, 25).

Similarly, in a *two* nanomagnet system [1], or in a complete *four* nanomagnet system using Bennett clocking [2], the out-of-plane excursion of magnetization needs to be considered as depicted in the Fig. 1(h). If magnetization gets deflected in so-called *bad* ϕ-quadrants, as explained in Refs. 2,6,7, the dipole coupling from the nanomagnet 1 [Fig. 1(h)] is not sufficient to switch the nanomagnet 2 in the correct direction, causing error in logic design. Ref. 1 considers only *in-plane* potential landscape while explaining, therefore it could not explain the primary reason behind the high error probability in magnetization switching for logic design purposes.

It should be noted that it is possible to harness more asymmetry in the system, rather than depending only on the out-of-plane excursion of magnetization [2,6,7], so that the sensing procedure and dynamic withdrawal of stress will not be required. As shown in Ref. 26, the interface and exchange coupling can create asymmetry in the system facilitating non-toggle switching, without any requirement of the sensing procedure.

(3) Ref. 1 uses a vague term 'interactive pulse timing' regarding Ref. 2. As explained in the above point, the strategy proposed in Ref. 2 is in line to the physical operation of the basic device operation, which Ref. 1 could not conceive. The pulse shaping methodology proposed in Ref. 1 is based on the understanding of *in-plane* motion and *not* on out-of-plane motion. Only in the very end of the paper, it

vaguely states that "provided the out-of-plane magnetization effects do not begin to dominate first." As explained in the above point, the contents in Ref. 1 lack the key understandings and analysis behind the critical device operation and high error probability.

(4) Ref. 1 states while referring Ref. 2 that "Unfortunately, the feedback circuit will dissipate so much energy that it defeats the very purpose of SML. It is therefore an ineffective countermeasure." Actually, the research presented in Ref. 1 is an ineffective countermeasure since it concludes that low error probability cannot be achieved for logic design with their proposal, i.e., pulse shaping. Moreover, it could not analyze the reasoning behind high error probability, which nonetheless exists in the literature [2].

Ref. 1 foretell *without any reasoning* that the sensing element will dissipate too much energy. It appears that the authors in Ref. 1 think that logic is limited to four magnet systems [5] and it would require charge-based transistors to build any other circuitry [27–31]. Such thinking misses the big picture involved. Note that researchers are trying to replace the traditional transistors by a new possible energy-efficient switch (e.g., using multiferroic composites). Therefore, any required circuitry in general can be built with the energy-efficient switch itself rather than using charge-based transistors. Usually, it requires several peripheral circuitry in addition to the basic switch itself and it does not change the orders of energy dissipation [32, 33].

As stated in Refs. 6,7, the sensing element to detect when magnetization reaches *around* $\theta = 90^\circ$ can be implemented with spin valve or magnetic tunnel junction, which is anyway required to read the magnetization state of a nanomagnet [23]. And it is well-known that a *small* magnitude of current is required to read the magnetization state, leading to only *miniscule energy dissipation*. Therefore, the comment made by Ref. 1 is untenable.

A few contradicting facts vis-a-vis the comment made by Ref. 1 are pointed out below.

(a) Ironically, a couple of authors in Ref. 1, Bandyopadhyay and Atulasimha (referred as BA onwards) are coauthors of Roy in Refs. 6,7,15–17. In particular, energy efficiency is claimed in the presence of thermal fluctuations in Ref. 17, which requires the sensing element too. Also, there is a patent [34] filed by BA including Roy's contributions [6,7,14–18] claims energy-efficiency requiring the sensing element therein as well. Therefore, the comment made by Ref. 1 is very perplexing.

(b) Note that Ref. 1 uses precisely shaped pulses. Such pulses need to be generated too using some circuitry. According to the perception of Ref. 1, transistors need to be utilized and the system would dissipate too much energy, invalidating the claim of energy efficiency in Ref. 1. Note that one additional hardware cannot be shared between many devices distributed on a chip due to interconnect

delay and loading effect. Also, note that pulse shaping is an ineffective countermeasure since it is not helping much in reducing the error probability, therefore building and using such circuitry do not make sense.

(c) Ref. 25, in which BA are coauthors, proposed a "toggle" switch (as stated that "a write cycle must be preceded by a read cycle to determine the stored bit"), which would require a similar use of spin-valve or MTJ for reading the known bit, storing it, and then using it for *comparison*. According to the perception of Ref. 1, such *additional* circuitry needs to be constructed with energy-inefficient transistors, invalidating the claim of energy efficiency in Ref. 25.

Fortunately, the perception in Ref. 1 is *incorrect*, otherwise, no system comprised of multiferroic devices would have been energy-efficient; transistors would have been required always to build the peripheral circuitry. Note that such sensing circuitry is not always required. It is shown in Ref. 26 that the interface and exchange coupling can create enough asymmetry in the system facilitating non-toggle switching, without any requirement of the sensing procedure and dynamic withdrawal of stress. Therefore, Ref. 1 misses several key understandings in this respect.

(5) Ref. 1 states while referring Ref. 2 that "We do not use any such construct and retain the energy advantage of SML." First, note that Ref. 1 fails to achieve high switching speed at tolerable error probability for logic design. Ref. 1 does *not* mention that the proposal in Ref. 2 achieves high switching speed ($\sim$1ns) at low error probability ($< 10^{-4}$) for logic design. The pulse shaping methodology in Ref. 1 cannot tackle the critical issue behind switching failures as analyzed in Ref. 2.

Apart from making incorrect and misleading statements on Ref. 2, Ref. 1 is erroneous in the following aspects.

(1) Ref. 1 states that "Since our voltage pulse widths are 1 ns or more, we can neglect effects associated with finite rise and fall times of the stress in response to an abrupt voltage pulse." Note that it is shown in literature [6, 7, 17] that particularly fall time is important to consider, since it may rotate magnetization out-of-plane in a direction that affects the error probability. Therefore, without a relevant analysis, the comparative basis of using different pulses (e.g., cases 3 and 4 pertain to ramped pulses, while the other cases do not) in Ref. 1 is untenable.

(2) Ref. 1 states that "Therefore, operating in the dipole dominated region reduces error rate but increases switching delay (because the stress is relatively weak), while operating at stress levels much above the dipole dominated region has the opposite effect." The comment that "operating in the dipole dominated region reduces error rate" is incorrect, since the error occurs while *withdrawing* the stress. If the magnetization's out-of-plane excursion is in so-called *bad* quadrant, it may be detrimental and magnetization may traverse in the opposite direction, as explained in Ref. 2. Therefore finite ramp rate particularly while withdrawing the stress is

necessary to consider. Ref. 1 did not consider finite ramp rate, which is not only unphysical but also very important for relevant quantitative analysis. The dipole coupling makes the potential landscape asymmetric and the degree of asymmetry is same irrespective of stress, which is symmetric. Such statement fails to identify the key issue that dipole coupling makes small asymmetry in the system herein. This is why dipole coupling cannot counter the motion due to out-of-plane excursion, as explained in Ref. 2, and thereby Ref. 1 pertains to a high error probability.

Also, "operating at stress levels much above the dipole dominated region has the opposite effect." is far from accurate since with high stress level accompanied by finite ramp rate, there can be considerable ϕ-motion [see Equation (1)] and precession, increasing the switching delay eventually [6, 7, 17].

(3) While explaining the peak in Fig. 5, Ref. 1 says that with the increase of stress "the influence of dipole interaction is diminished" etc. This is not a correct explanation since asymmetric dipole coupling is always active alongwith the symmetric stress [see Fig. 1(i)]. For a correct explanation, one needs to invoke the out-of-plane excursion of magnetization with stress amplitude and stress pulse timing as parameters, as explained in Ref. 2.

(4) Ref. 1 states incorrectly that "Any combination of a, b and t that gives a barrier height of 32 kT will yield similar results." Note that the demagnetization factors dictate the magnetization dynamics and they depend on the specific values of a, b and t. For example, switching delay can vary twice or more for the same barrier height [35]. This is a basic understanding regarding magnetization dynamics. Also, the barrier height needs to be calculated accurately. Several papers [21, 24, 25] underestimated the barrier height as much as by 40% using the assumption $a/b \sim 1$.

(5) Ref. 1 does not provide a correct mathematical procedure to calculate the critical stress in the presence of dipole coupling. It uses a stress of 3 MPa [rather than 2.64 MPa, calculated with a relevant procedure, see Fig. 1(i)], which does *not* make minimum energy position at the easy axis.

(6) There are less serious but confusing and erroneous issues in Ref. 1, e.g., Equations (7)-(9) should have "3λ" in stead of "2λ" (sometimes λ_s is used for λ), the calculated values of Equations (8) and (9) correspond to $d = 200\,nm$ instead of $d = 150\,nm$, in Fig. 4, θ (instead of ϕ) is used as azimuthal angle, there are two Fig. 4(c)s in the plot, Figs. 6, 8, and 10 plot ϕ from $-\pi$ to 2π, while ϕ has a range of only 2π and it therefore depicts some duplicate and separated distributions incorrectly, also it appears that the last set in the Figs. 6, 8, 10 corresponds to 2 ns rather than 3 ns etc.

While there exists a litany of errors in Ref. 1, the purpose of this Comment is to primarily point out that Ref. 1 has made *incorrect* statements on Ref. 2 as explained earlier: (1) misquoted that Ref. 2 deals with memory and not logic, (2) did not mention that the proposal in Ref. 2 can keep the switching speed high $\sim$1 ns alongwith low error probability, unlike the case in Ref. 1, and (3) made *misleading* statement that energy

dissipation in Ref. 2 is high. The understandings reflected in Ref. 1 are incorrect and *not* sound, while predicting the demise of multiferroic nanomagnetic logic in the presence of thermal fluctuations [1, 4, 5, 36, 37].

It should be also pointed out that there is issue with scaling down device dimensions since the analysis performed in Ref. 1 depends on the *in-plane* asymmetry created by dipole-coupling (between laterally placed nanomagnets), which decreases with scaling. Therefore, in the scaled-down nanomagnets, the error-probability would be even higher than what is mentioned in Ref. 1. There is also similar issue regarding *area consumption* on the proposals in Refs. 24, 25 due to using *lateral* piezoelectric pads, which is tantamount to *micro*-electronics rather than *nano*-electronics [12, 13], and therefore untenable for meeting practical standard requirement of area density 1 Tb/in^2. Both theoretical and experimental works are emerging in this area [38] and the issues pointed out here hopefully would play an important role in devising memory and logic in our future information processing systems.

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Comment on "An error-resilient non-volatile magneto-elastic universal logic gate with ultralow energy-delay product" [Sci. Rep. 4, 7553 (2014)]

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An article[1] by Biswas and the coauthors Atulasimha and Bandyopadhyay (referred as BA onwards) claimed to devise an error-resilient and ultralow energy universal logic gate NAND using piezoelectric-magnetostrictive heterostructures. Here it is pointed out that the basic idea behind such gate using piezoelectric-magnetostrictive heterostructures with multiple inputs is followed from Ref. 2. The Ref. 1 pertains to neither error-resilient nor energy-efficient operation, which follows from BA's own contention. Moreover, the statements made in the Ref. 1 on Ref. 2 are incorrect and misleading. Furthermore, the proposal in Ref. 1 is highly area-consuming and lacks scalability, contrary to what is claimed in the article. There are other technical issues too in Ref. 1, as pointed out here.

First, note that Ref. 1 uses a $\sim 90^\circ$ (precisely 86.4°) switching mechanism following an earlier idea by others[3–6]. Therefore, *magnetization does not switch a complete* 180° in Ref. 1 and this leads to a low tunneling magnetoresistance (TMR) while reading the magnetization state and it has serious consequence on *read* error probability. The researchers are in fact trying to increase the TMR using half-metals (rather than using CoFeB) to avoid high read-error rate, so lowering the angular separation to 90° (from 180°) is an important issue in Ref. 1.

Next, BA's comments on Ref. 2, which follows a complete 180° switching mechanism[7,8], are factually and technically incorrect and misleading, as explained here. BA state that it requires a sensing circuitry for operation of the proposal in the Ref. 2 and indicates as if it is an issue with the computing proposal in Ref. 2. First, BA do not point out at all that the sensing element is required for complete 180° switching only and it does not require so if 90° switching mechanism is used, as BA have used in Ref. 1. Second, Ref. 2 just uses the existing complete 180° magnetization switching methodology[7–10]. In Ref. 2, it is clearly mentioned while referring the Ref. 7 that "Computing methodologies utilizing such 180° switching mechanism between the two stable states of a shape-anisotropic magnetostrictive nanomagnet have not been proposed so far." The computing proposal in Ref. 2 is based on the switching methodology explained in the Ref. 7 (and also Refs. 8–10) and it was stated in the Ref. 2 clearly.

In Ref. 11, BA comment that the sensing circuitry for magnetization switching (complete 180°) to dissuade thermal fluctuations "will *likely* require multiple charge-based electronic devices (e.g. transistors) that are known energy hogs" is diffident, misses the basic understanding level, and completely contradicts the big picture involved. Note that researchers are trying to replace the traditional *switch* based on charge-based transistors by a new possible "ultra-low-energy" *switch* (e.g., using multiferroic composites). Therefore, any circuitry can be built with the energy-efficient switch itself rather than the conventional transistors. Usually, it requires several peripheral circuitry in conjunction with the basic switch in a system[12,13]. While researchers report on the performance metrics of the basic switch itself, the total energy dissipation considering the other required circuitry does not change the order of energy dissipation, utilizing the respective devices[12,13]. This was the understanding while claiming energy-efficiency in Ref. 8, where BA are coauthors. Therefore, BA's contention that the computing methodology in Ref. 2 cannot pertain to "ultra-low-energy" operation due to the underlying magnetization switching methodology is untenable and violates the ethical policy of coauthorship[14] ("Any individual unwilling or unable to accept appropriate responsibility for a paper should not be a coauthor."). Moreover, BA conceived such understandings from Roy[7], which makes the BA's comments[11] devoid of any scientific reasoning in this respect. Several new ideas on the switching methodology exerting more asymmetry in the system may come along too, e.g., interface and exchange coupled systems, as evaluated in Ref. 15 by Roy, which would not require any sensing circuitry and also it can maintain the direction of switching unlike toggle switching[7,16].

As stated in the Ref. 7, the sensing circuitry to dissuade thermal fluctuations can be implemented by measuring the magnetoresistance in a spin-valve or magnetic tunnel junction (MTJ), which needs to be used anyway to *read* the magnetization state and it dissipates much less energy than for *write* operation. We know the magnetoresistance of the MTJ when magnetization resides at nanomagnet's hard-plane and comparing this known signal with the sensed signal of the MTJ, the stress can be ramped down[7]. Such comparator can be implemented with these energy-efficient multiferroic devices, i.e., charge-based transistors do not need to be utilized. Moreover, the fabrication procedure of transistors and nanomagnets are different, therefore, it is beneficial to use the same device throughout rather than having layers of different devices with different fabrication procedures.

Note that there are inconsistencies in the Ref. 1 coauthored by BA while comparing their Comment[11]. In

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their Comment[11], BA state "charge-based electronic devices (e.g., transistors) that are known energy hogs", however, note that in Ref. 1, BA state that "a low-power transistor may dissipate only 10^3 kT of energy when it switches in 0.1 ns (energy-delay product = 3×10^{-28} J-s)". The key point is that there exists switching delay-energy trade-off in devices, i.e., if a device is switched slower, it dissipates a lower energy. Therefore, if transistors were to switch slower, the energy dissipation could have been much lower. Ref. 2, on which BA's Comment[11] is based, pertains to switching delay of ∼1 ns, therefore even if transistors are utilized to build any additional hardware (however, this is a misconception as described above), then energy dissipation would not have been issue, contrary to BA's own claim.[11] The challenge is to reduce energy dissipation of a device while keeping the switching delay intact[17]. There can be other metrics like area and error-probability in the trade-off analysis too. BA's Comment[11] did not take such trade-off into consideration while defining transistors as energy hogs and commenting on Ref. 2. Anyway, as mentioned earlier, the charge-based transistors need not be used to build any additional hardware, rather multiferroic devices themselves can be utilized.

Ironically, Ref. 18, in which BA are coauthors, proposed a "toggle" switch (as stated that "a write cycle must be preceded by a read cycle to determine the stored bit"), which would require a similar use of spin-valve or MTJ for reading the known bit, storing it, and then using it for *comparison*. According to BA's own contention[11], such *additional* circuitry needs to be constructed with energy-inefficient transistors, invalidating the claim of energy efficiency in Ref. 18. Also, Ref. 19, in which BA are coauthors, uses some pulse shaping methodology (which, however, leads to "high" error probability at high switching speed that is required to build general-purpose nanoelectronics[20,21]). According to BA's own contention[11], the circuitry for generating the precisely shaped pulse needs to be constructed with energy-inefficient transistors, invalidating the claim of energy efficiency in Ref. 18. (Note that one additional hardware cannot be shared between many devices distributed on a chip due to interconnect delay and loading effect.) Therefore, BA are contradicting their own Comment[11], however, incorrect and misleading.

Similarly, in Ref. 1, according to BA's own contention[11], the current source I_{BIAS} and resistors would need to be built with transistors invalidating the claim of energy efficiency in Ref. 1. According to BA's contention[11], in a system, any circuitry other than the basic switch itself needs to be constructed with energy-inefficient transistors and in this way no system based on nanomagnetic logic would be energy-efficient. (Note that one current source I_{BIAS} cannot be shared between many devices distributed on a chip due to interconnect delay and loading effect.) However, this is incorrect since BA missed the basic understanding level here as explained beforehand. Note that BA did not complain on such energy-inefficiency in papers on magnetization switching methodology[8] where they are coauthors.

BA talks about nanosecond switching speed of the device in Ref. 1. Interestingly, such nanosecond switching delay cannot be conceived by considering only the in-plane potential landscapes of magnetization (Figs. 2 and 3 in Ref. 1). Magnetization may deflect out of magnet's plane when stress is applied since the torque due to stress acts in the out-of-plane direction as

$$\mathbf{T_{E,stress}} = -\hat{\mathbf{e}}_\mathbf{r} \times \nabla E_{stress} = -(3/2)\,\lambda_s \sigma \Omega sin(2\theta)\,\hat{\mathbf{e}}_\phi, \quad (1)$$

where $E_{stress} = -(3/2)\,\lambda_s \sigma \Omega cos^2\theta$ is the potential energy due to stress, $(3/2)\lambda_s$ is the magnetostrictive coefficient, σ is the stress, Ω is nanomagnet's volume, θ and ϕ are polar and azimuthal angles in spherical coordinate system [represented by (r,θ,ϕ)], respectively[17]. Therefore, *magnetization rotates out-of-plane* even if the demagnetization factor in the out-of-plane direction is high (∼10 times compared to the in-plane directions). A slight out-of-plane excursion has important ramification to increase switching speed tremendously[7–10], which cannot be conceived if magnetization is *assumed* to reside always on magnet's plane as *assumed* by BA in Ref. 22 unreasonably. If we calculate the switching delay of magnetization according to Ref. 22, it will incorrectly come out as ∼1000 ns, which is clearly exorbitantly high for general-purpose applications[20,21]. Therefore, Ref. 22 would have been *untenable to build general-purpose nanoelectronics*. If charge based transistors were to operate *slow*, the energy dissipation would not have been an issue[12,20,21]. However, the analysis in Ref. 22 is incorrect. Stress rotates magnetization out of magnet's plane and this generates a helpful torque that rotates magnetization *fast*, increasing the switching speed to more than 1 GHz[7–10]. This was first *corrected* by Roy in Refs. 9 and 23, which put the nanomagnetic memory and logic based on multiferroic composites on solid footing[17]. Such key idea by Roy and associated papers[7–10,23] have been utilized by BA in a patent[24]. But, BA are complaining[1,11] over the very same magnetization switching methodology used in Ref. 2 by Roy.

There are two more misleading statements in Ref. 1 on Ref. 2. In Ref. 11, BA agreed that with the help of a sensing circuitry, the error-resiliency can be achieved for the proposal in Ref. 2, which was already lucidly explained by Roy in Ref. 7. However, in Ref. 1, BA comment that the proposal in Ref. 2 is error-prone *as well as* mentioning of the sensing circuitry needed for error-resilient 180° switching[7]. The sensing circuitry is used for error-resilient switching.[7] Therefore, stating both sensing circuitry and error-prone (in Ref. 1 by BA) is categorically incorrect and misleading.

Also, BA comment in Ref. 1 that the design in Ref. 2 is flawed while referring their Comment[11], which is factually and technically incorrect and misleading. On design issues, BA raised a couple of incorrect issues on Ref. 2 in their Comment[11]. First, BA argue that the stresses generated by the two inputs do not add in magnitude.

This is *incorrect* and *misleading*. The inputs generate *strain* in the piezoelectric layer and each input generates a same strain. (Note that the inputs are *symmetrically* placed on the piezoelectric layer.) The addition of strains due to two inputs can be simply understood from the superposition principle for a linear system (strain is proportional to the electric field[7–10]). Any detailed solver with underlying detailed equations can confirm that too[25]. The response of the system is strain and electric field is the input to the system. One should not consider the charge in the Poisson's equation since these are *strain-mediated* multiferroic composites[2,7–10,26] and not the charge-mediated ones.

Second, BA raised an issue on the concatenation between the individual devices and that is incorrect and misleading too. Note that concatenation in Ref. 2 is addressed and it is clearly mentioned that "The SET operation precedes the LOGIC operation ..." which BA did not take into account. For an individual gate, it needs to perform a SET operation *before* going for LOGIC operation *on that gate*. A voltage on the "Set" terminal is applied to perform the SET operation, which is stated in the paper. BA are *not* considering this (note that there are no SET inputs in the Fig. 1 of the Comment by BA[11]) and hence this is a factually incorrect and misleading point raised by BA.

Note that Ref. 1 has a very high *read* error probability, which is a consequence of using a 90° switching mechanism, contrary to complete 180° switching mechanism used in Ref. 2. Following Ref. 1, in the high logic state, a 5% variation of input voltage is intolerable and fails the logic operation. Therefore the error-resiliency claim in the Ref. 1 is severely flawed.

Also, the claim and notion of scalability discussed in Ref. 1 are flawed. Equation (1) clearly says that the stress anisotropy is proportional to the volume of the nanomagnet. This is similar to magnetic field based switching, i.e., at a lower volume of the nanomagnet, it requires a higher stress (and a higher voltage that generates the stress) to produce the same stress anisotropy. Unless additional strategies are incorporated, the claim of scalability in Ref. 1 is untenable. The other properties stated for logic operation in Ref. 1 are *not* new in literature.

In Ref. 27 (which is referred in Ref. 1), BA predicated the demise of Bennett clocking mechanism in the presence of room-temperature thermal fluctuations saying "This could render nanomagnetic logic schemes that rely on dipole coupling to perform Boolean logic operations." But the critical analysis performed in Ref. 26 says otherwise. Ref. 26 showed that the out-of-plane excursion of magnetization (which was missed by BA in Ref. 22) combined with the thermal fluctuations is the reason behind switching failures and BA failed to grasp such understanding in Ref. 27 and thereby incorrectly predicting the demise of general-purpose nanomagnetic logic. Note that Ref. 19, in which BA are coauthors, is error-prone at high switching speed and therefore the operation at low switching speed (∼10 MHz) is untenable for building general-purpose nanoelectronics, while for niche applications it still needs to compete with the existing transistor based technology, which is energy-efficient at low switching speed.

Note that Ref. 2, on which BA's Comment[11] is based, presents a novel intriguing methodology of building logic rather than Bennett clocking mechanism using multiferroic composites[17,23], i.e., using a single device with a read-unit (MTJ) as a *switch* (similar to that a transistor acts as a *switch*). Also, it is shown in Ref. 2 how to increase the *functionality* per device, e.g., it proposed universal logic gates (NAND and NOR) utilizing a *single* device with the well-established concept of using multiple contacts on the device to add up the strains generated in piezoelectric[25], and a *Set* input to preset the non-volatile magnetization state and facilitate concatenation, which are not conceived by BA in their Comment[11]. Note that it is advantageous to increase the *functionality* per *single* device since stress anisotropy generated in the magnetostrictive nanomagnets is proportional to nanomagnet's volume and therefore, these *single* multiferroic devices are area-inefficient. Hence, the proposal in Ref. 2 can facilitate a highly-dense yet an ultra-low-energy computing paradigm. In Ref. 1, the authors follow the same principles as in Ref. 2.

Ref. 1 uses resistors and potential divider (see Fig. 1 in Ref. 1) to accommodate multi-inputs. The resistors need to be implemented additionally and would consume area. Comparatively, the device design in Ref. 2 uses *intrinsic* strain-addition property of piezoelectrics. The *external* manipulation of inputs in Ref. 1 is a matter of concern. Note that such external way of using multi-inputs can be also used for traditional transistors to build universal logic gates, but it is not done, rather multiple transistors are used. It is stated in Ref. 1 (in the supplementary material) that "The dissipation in the resistance R can be negligible as we can make this resistance arbitrarily high." This is incorrect (any standard electrical engineering undergraduate textbook can be consulted) since RC delay may be too high. Therefore, such design proposed in Ref. 1 is untenable.

There are some other technical flaws in Ref. 1 too. Ref. 1 says that the hard nanomagnet in the fixed layer is *not* magnetostrictive. However, the hard nanomagnets in the fixed layer (synthetic antiferromagnetic layer) are usually made of CoFeB, which is magnetostrictive. Also, stress is unreasonably assumed to be removed abruptly in Ref. 1, however, it was shown by Roy[7,8] that finite ramp rate of stress has immense consequence on magnetization dynamics particularly it can cause switching failures in the presence of thermal fluctuations. Also, Ref. 1 incorrectly states that the resistance changes by *twice* using a wrong equation[16] (while additionally *assuming* 100% spin injection/detection efficiencies) for the 90° switching mechanism used therein. Moreover, Ref. 1 incorrectly calculated the demagnetization factors and the energy barrier height for a nanomagnet with the assumption of major axis (a)/minor axis (b)∼ 1 (while

a/b=100 nm/42 nm), which is very unreasonable. Furthermore, the design proposed in Ref. 1 (also in Refs. 16 and 18) is highly area-consuming due to using lateral piezoelectric pads. There is an ongoing drive to reduce the area-consumption[15,28], but Refs. 1, 16, and 18 took such drive backwards.

Note that Ref. 16 (the authors are same as of in Ref. 1) claimed a superior design of magnetoelastic memory (incomplete non-180° switching of magnetization), compared to an earlier idea[3–6]. The results presented in Ref. 16 are, however, incorrect and actually the switching delay and error-probability are inferior to the earlier idea[3–6]. In the Ref. 1, note that BA have utilized the magnetization switching methodology as in the Refs. 3–6. If Ref. 16 performs better than Refs. 3–6, then BA simply could have utilized the switching methodology in Ref. 16 for the logic design in Ref. 1.

Finally, note that Fig. 4 in the Ref. 1 showing gain in the system is already there in literature. Ref. 29 first states about the voltage amplification, i.e., gain with the procedure to evaluate that. Such characteristics (Fig. 4 in the Ref. 1) has been already reported in literature (see Fig. 4(b) in Ref. 30 and Fig. 5(b) in Ref. 31). However, Ref. 1 does not mention the references[29–31].

To summarize, the central claims and analysis of the Ref. 1, while following Ref. 2, are flawed. The *incomplete* 90° switching mechanism is an issue behind the high *read* error rate in Ref. 1. Ref. 1 provides *misleading* statements on Ref. 2, which uses a complete 180° switching methodology. BA have repeatedly failed to conceive the key understandings, e.g., magnetization is unreasonably *assumed* by BA to be confined on magnet's plane[22], which has key consequence on magnetization dynamics underestimating the switching speed tremendously[7,17] and causing issues in regards to error probability at room-temperature analysis[26]. Incorrectly, BA have also predicted the demise of nanomagnetic logic[27]. And, most recently, in Ref. 1, BA have also come up with misleading statements on Ref. 2, as explained here. Both theoretical and experimental efforts are emerging in this field of research on further improving the performance metrics and the *comprehensive* discussion clearing the facts here would hopefully play an important role in possibly devising the magnetization switching methodology and nanomagnetic logic.

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Response to "Comment on "Ultra-low-energy non-volatile straintronic computing using single multiferroic composites"" [Appl. Phys. Lett. 103, 173110 (2013)]

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In a Comment,[1] Bandyopadhyay and Atulasimha (referred as BA onwards) allege that the proposal in Ref. 2 cannot pertain to "ultra-low-energy" and "non-volatile". First, no issue has been raised regarding the "non-volatile" operation surprisingly. Second, in the context of "ultra-low-energy" computing, BA's statements are factually and technically incorrect, as explained below.

BA state that it requires a circuitry to dissuade room-temperature thermal fluctuations for the proposal in Ref. 2, which is "first" mentioned in Ref. 3 and not beforehand. This is factually incorrect since it is already explained in Ref. 4 as BA are aware of. In Ref. 2, it is clearly mentioned while referring the Ref. 4 (Ref. 5) that "Computing methodologies utilizing such 180° switching mechanism between the two stable states of a shape-anisotropic magnetostrictive nanomagnet have not been proposed so far." The computing proposal in Ref. 2 is based on the switching methodology proposed in the Ref. 4 and it was stated in the Ref. 2 clearly. As BA would be aware of, being coauthors of Roy, there were already several other papers on such switching methodology.[4–8]

BA's comment that the sensing circuitry "will *likely* require multiple charge-based electronic devices (e.g. transistors) that are known energy hogs" completely misses the big picture. Researchers are trying to replace the traditional *switch* based on charge-based transistors by a new possible "ultra-low-energy" *switch* (e.g., multiferroic composites) and there are several centers funded by national agencies over such research. Therefore, any circuitry can be built with the energy-efficient switch itself rather than the conventional transistors. Usually, it requires several peripheral circuitry in conjunction with the basic switch e.g., access transistors, sense amplifiers etc. for the design of static random-access-memory (SRAM) cells using transistors. While researchers report on the performance metrics of the basic switch itself, the total energy dissipation considering the other required circuitry does not change the order.[8–10] This was the understanding while claiming energy efficiency in Ref. 8, where BA are coauthors. Also, there is a patent[11] filed by BA including Roy's works[4–8,12,13] that claims energy-efficiency requiring the sensing element therein as well. Therefore, the comment made by Ref. 1 is very perplexing.

Next, BA's contention that it requires to withdraw the stress *as soon as* magnetization comes to the hard-plane is factually incorrect as the analysis performed in Ref. 4 says otherwise that there exists tolerance due to inherent magnetization dynamics. Stress rotates magnetization out of magnet's plane and it generates an *intrinsic asymmetry*, which directs magnetization to switch in the correct direction,[4] and it cannot be conceived by confining magnetization on magnet's plane as *assumed* by Ref. 14. In Ref. 15, BA concede the very same concept of a sensing/feedback circuitry that the magnetization state needs to be read and then the information needs to be fed to the stress generator to exert the stress again. Such "toggle" switch (not a proper memory) as claimed by Ref. 15, apart from being highly area-consuming, cannot operate quite reliably due to ramp-rate effect, which is not considered, but that is critical to the magnetization dynamics as explained in Ref. 4. Using spin-transfer-torque switching mechanism to maintain the direction of a toggle memory[15] would dissipate energy several orders of magnitude more[16] than the current charge-based transistor technology. Also, there is a proposal of incomplete switching ($< 180°$) of magnetization.[17] Memory of non-toggle type and complete 180° switching is proposed in Ref. 18 recently. The polarization-magnetization coupling generates asymmetry and in this case there is no need for any sensing circuitry even in the presence of thermal fluctuations.[18] There can be different switching mechanisms, but it does not affect the significance of the study presented in the Ref. 2.

BA's contention that the Ref. 3 concedes for the first time the requirement of the sensing circuitry, which as explained above is factually incorrect. It is already mentioned and explained in the Ref. 4, as BA are aware of. BA's comment that "magneto-tunneling junctions (MTJ) and resistance sensors" is energy-dissipative is incorrect since the whole community knows that reading information via MTJs pertains to much less energy dissipation than that of writing information, which is why only the switching of magnetization is taken into account while calculating the energy dissipation. The Ref. 3 deals with the Bennett clocking mechanism for logic design purposes, in which there is already an asymmetry-making field from the neighboring nanomagnets due to dipole coupling that can switch the magnetization in the correct direction. However, detailed critical analysis in the presence of room-temperature thermal fluctuations reveals that the magnitude of this asymmetry-making field is not sufficient to achieve enough low error probability

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for computing purposes.[3] Hence, the asymmetry-making field due to out-of-plane excursion of magnetization, as explained in the Ref. 4, is brought into account and suggested as a remedy. Several new ideas on the switching methodology exerting more asymmetry in the system may come along too (e.g., see Ref. 18). In Ref. 19, BA predicated the demise of Bennett clocking mechanism saying "This could render nanomagnetic logic schemes that rely on dipole coupling to perform Boolean logic operations." But the critical analysis performed in Ref. 3 says otherwise.

Next, BA raised a couple of issues more. First, BA argue that the stresses generated by the two inputs do not add in magnitude. This is not correct. The inputs generate *strain* in the piezoelectric layer and each input generates a same strain. (Note that the inputs are *symmetrically* placed on the piezoelectric layer.) The addition of strains due to two inputs can be simply understood from the superposition principle for a linear system (strain is proportional to the electric field[4–8]). Any detailed solver can confirm that too. The response of the system is strain and electric field is the input to the system. One should not consider the charge in the Poisson's equation as BA are implying since these are *strain-mediated* multiferroic composites[2–8] and not the charge-mediated ones.

Second, BA raised an issue on the concatenation between the individual devices and it is incorrect too. In the Letter,[2] it is clearly mentioned that "The SET operation precedes the LOGIC operation ..." which BA did not take into account. For an individual gate, it needs to perform a SET operation before going for LOGIC operation *on that gate*. A voltage on the "Set" terminal is applied to perform the SET operation, which is stated in the paper. BA are *not* considering this and hence this is a factually incorrect issue raised by BA.

BA allege that the claims in the Letter did not pass scrutiny. The above response explains that the issues are factually and technically incorrect and misleading.

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Comment on "Complete magnetization reversal in a magnetostrictive nanomagnet with voltage-generated stress: A reliable energy-efficient non-volatile magneto-elastic memory" [Appl. Phys. Lett. 105, 072408 (2014)]

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In Ref. 1, Biswas and the coauthors Bandyopadhyay and Atulasimha (referred as BA onwards) claimed a reliable and energy-efficient way of "toggle" switching of magnetization in piezoelectric-magnetostrictive heterostructures. Here we show that the analysis is incorrect and furthermore the device is highly area consuming and of low switching speed. For such "toggle" switching, since a write cycle must be preceded by a read cycle to determine the stored bit, extra circuitry would be required. According to BA's own contention, such *additional* circuitry needs to be constructed with energy-inefficient transistors, invalidating the claim of energy efficiency.

Ref. 1's claim of reliability of switching is based on the unreasonable assumption that the stress is "instantaneous". The argument in Ref. 1 that "Since the piezoelectric response of PZT is much faster than the magnet switching, we can view the strain generation as instantaneous." is incorrect. It has been shown[2,3] that even ∼100 ps ramp duration, which is smaller than magnetization switching delay (∼1 ns) has profound impact to cause switching failures. Stress rotates magnetization out of magnet's plane (unlike incorrectly assumed that the magnetization always stays on magnet's plane in Ref. 4) and this can cause magnetization to backtrack resulting in switching failures.[2] Therefore, when magnetization switches in three steps ($A \rightarrow B$, $B \rightarrow C$ and $C \rightarrow D$ in Fig. 1), the *finite* ramp rate of stress in each step *must* be considered to claim *reliability* on successful switching.

Also, Fig. 1 depicts how switching delay is required to be increased by a considerable extent due to 3-step switching strategy[1] to satisfy a given error probability. Fig. 1(b) shows a typical switching delay distribution[2,3] and the tail of such distribution determines the error probability. Since Ref. 1 proposes the 3-step procedure for switching, it *requires* to provide enough time to *every* step to conform to a given error probability. This increases the switching delay *tremendously* as the error probability is lowered. Moreover, the "toggle" switching[1] *requires* a read cycle to determine the stored bit and the ∼100 MHz switching speed (contrary to 1 GHz switching speed mentioned in the abstract)[1] obtained is clearly untenable for building nanoelectronics.[5,6]

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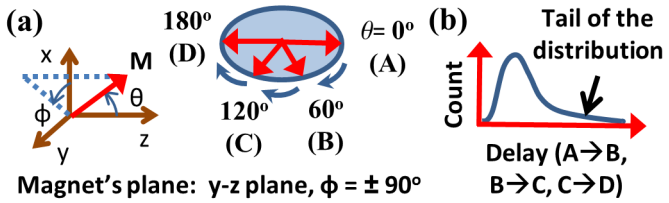

FIG. 1. (a) Magnetization switches in three steps, $A \rightarrow B$, $B \rightarrow C$, and $C \rightarrow D$. (b) A typical distribution of delay for each step.

The "toggle" switching proposed[1] requires *additional* circuitry to read the stored bit and *comparing* it to the desired bit to write. Ref. 1 neither explicitly mention the requirement of such circuitry nor refer to any other references. Recently, BA conceded that any such circuitry is *required* to be built by "multiple charge-based electronic devices (e.g., transistors) that are known energy hogs".[7] Therefore, according to BA's own contention, the proposal in the Ref. 1, contrary to the claim in the title itself, will be very energy-inefficient. However, the perception of BA in Ref. 7 is incorrect. Usually it requires additional circuitry in conjunction with the basic device itself, and considering the dissipation in the additional circuitry does not change the order of energy dissipation *using the respective devices*.[2,3,8,9]

Complete switching of magnetization in piezoelectric-magnetostrictive heterostructures exploiting the out-of-plane excursion of magnetization has been proposed earlier.[2,3,10,11] We can use a sensing element to detect when magnetization polar angle θ reaches *around* 90°, so that we can ramp down the stress thereafter.[2] There is tolerance however, i.e., θ does not need to be at *exactly* the right juncture 90°,[2] unlike incorrectly stated in Ref. 1. Since we already have a spin-valve or magnetic tunnel junction (MTJ) measuring the magnetoresistance to *read* the magnetization state, which dissipates much less energy than for *write* operation, we can utilize it to build the sensing element.[2] Comparing with the known value of the magnetoresistance when magnetization resides at $\theta = 90°$, the stress can be ramped down.[2] Any such circuitry can be built with these piezoelectric-magnetostrictive heterostructures acting as a *switch*. Also, such switching methodology in Refs. 2 and 3 has been analyzed to be able to cope with finite ramp rate *reliably*, unlike the case in Ref. 1, where unreasonably instantaneous ramp

is *assumed*.

Ref. 1 uses lateral pads on the piezoelectric of dimensions 120 nm/80 nm, which makes it highly area-consuming. There is ongoing drive to reduce area of devices to build nanoelectronics,[12,13], however, Ref. 1 took such drive backwards. There is proposal of *incomplete* switching of magnetization,[14] which is also area consuming for the very same reason. Such issue on area and low switching speed are not taken into consideration in Ref. 1 while comparing to spin-transfer-torque switching. Also, multiple voltage terminals need to be connected per device in Ref. 1 adding overhead to the system.

Note that although stress anisotropy is proportional to the volume of the magnetostrictive nanomagnets, the area consumption issue can be tackled by increasing the *functionality* per device, e.g., Ref. 15 proposed universal logic gates (NAND/NOR) utilizing a *single* device with the well-established concept of using multiple contacts on the device to add up the strains generated in piezoelectric,[16] and a *Set* input to preset the non-volatile magnetization state and facilitate concatenation, which are not conceived by Ref. 7. Also, unlike *toggle* switching, it is shown that interface magnetoelectric effect and exchange coupling can maintain the direction of switching[13] without requirement of any sensing circuitry[1,2] alongwith promising performance metrics for area, delay, and energy dissipation *simultaneously*. Such switching methodology can be utilized for building logic too.[15,17] With the emerging experimental efforts, the theoretical key concepts described here would play a crucial role in possibly devising the switching methodology and nanomagnetic logic.

Also, the energy barrier height calculated in Ref. 1 is underestimated by $\sim$40% using the *assumption* of $a/b \sim 1$ (while a/b=110 nm/90 nm) and the reference 8 referred in Ref. 1 is *not* on topological insulators as incorrectly indicated.

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Comment on "Energy-efficient magnetoelastic non-volatile memory" [Appl. Phys. Lett. 104, 232403 (2014)]

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Ref. 1 claimed a superior design of magnetoelastic memory, compared to an earlier idea.[2–5] Here we show that the analysis is incorrect and there are several technical issues in the Ref. 1. Furthermore the design proposed in Ref. 1 is highly area-consuming, invalidating any claim of a superior design.

First of all, Ref. 1 calculated the demagnetization factors for a nanomagnet with the assumption of $a/b \sim 1$ (while a/b=110 nm/90 nm, underestimating the energy barrier by ∼25% and a/b=150 nm/63 nm, underestimating the energy barrier by ∼50%). However, these incorrect data are utilized for pointing further incorrectness to communicate the issues on similar ground. Comparatively, the lateral area chosen by Ref. 1 is an order higher than that of chosen by Ref. 2. This is a serious issue and untenable for building nanoelectronics.[6,7] Also, Ref. 1 chooses to use two pairs of electrodes, which consume *additional large area* for *each* nanomagnet apart from the area consumption by the nanomagnet itself. There is an ongoing drive to reduce the area-consumption,[8,9] but Ref. 1 took such drive backwards.

Fig. 1(a) shows the nanomagnet's potential landscape for the proposal in Refs. 2–5 *assuming* the incorrect parameters chosen by Ref. 1. It depicts how magnetization can be switched (from $\theta = 135°$ to $\theta = 45°$) with the application of stress (similar to Fig. 3 in Ref. 4). Fig. 1(b) shows the nanomagnet's potential landscape in Ref. 1 with two pairs of electrodes AA' and BB'. Switching (from $\theta = 155.9°$ to $\theta = 24.1°$) in this case happens in two steps $A \rightarrow B$ and $B \rightarrow C$. Since we need to take care of the *tail* of the switching delay distribution in the presence of thermal fluctuations representing the worst case error probability that is needed to satisfy, we must give enough time for *each* of the two steps so that all the trajectories switch successfully. This increases the switching delay tremendously for the case in Ref. 1 with the lowering of the error probability.

Figs. 1(c) and 1(d) depict one illustrative switching failure in Ref. 1. Note that magnetization azimuthal angle ϕ gets deflected from 90° (along which a magnetic field is exerted). Depending on the *direction* of deflection around $\phi = 90°$, it may aid or hinder the rotation of polar angle θ.[10–12] Such out-of-plane excursion was *not* considered in Ref. 13, however, it has a critical significance at finite temperature analysis and on increasing the switching speed significantly.[10–12] Fig. 1(c) shows that even if stress is withdrawn as late as at 1.5 ns, magnetization

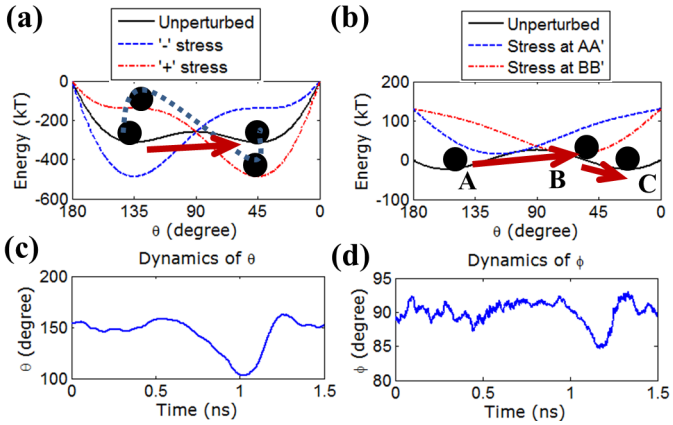

FIG. 1. (a) Nanomagnet's potential landscape (in-plane, $\phi = 90°$) for the proposal in Refs. 2–5. (b) Nanomagnet's potential landscape (in-plane, $\phi = 90°$) for the proposal in Ref. 1. (c) An illustrative switching failure for the case in Ref. 1. Dynamics of polar angle θ. (d) Dynamics of azimuthal angle ϕ.

fails to switch and *backtracked* towards $\theta = 155.9°$. Also, slow ramp rate of stress can cause switching failures,[10] however, Ref. 1 *assumed* the ramp rate unreasonably instantaneous. The kind of switching failure due to *backtracking* is not quite applicable for the case in Refs. 2–5, and Ref. 1 missed it completely while comparing the error probability. Some switching trajectories may be very close to the destination [$\theta = 45°$ in Fig. 1(a)] and this should not be deemed as switching failures.[2–5] Therefore, Ref. 1 has worse error probability, however, it is claimed otherwise. Also, Ref. 1 needs to rotate magnetization at a larger span of $155.9° - 24.1° = 131.8°$ compared to $135° - 45° = 90°$ for the proposal in Refs. 2–5. It turns out from the simulation results that the switching delay for the proposal in Ref. 1 is actually higher, however, it is claimed otherwise.

Ref. 1 has a serious problem in grasping the *symmetry* in the system as it states the stable states *asymmetric* (e.g., $\theta = 155.9°$ and $\theta = 24.09°$, and $\theta = 46°$ and $\theta = 134.5°$). Also, Ref. 1 calculates incorrectly the error probability due to *random* thermal fluctuations for the proposal in Refs. 2–5 (not due to *backtracking* as in Ref. 1) quite *different* for $135° \rightarrow 45°$ and $45° \rightarrow 135°$ switching in the *symmetric* landscapes shown in the Fig. 1(a) without explaining any reason behind it.

Note that it requires *four top contacts* to be made *for each nanomagnet* for the proposal in Ref. 1, which adds overhead on the power grid and is not considered while

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comparing the energy dissipation. Also, simulation results say that a lower stress (i.e., a lower voltage decreasing the energy dissipation) than 19.5 MPa can switch magnetization for the proposal in Refs. 2–5. Decreasing stress will increase switching delay (note the switching delay is actually higher in Ref. 1 comparatively), but will reduce the energy dissipation. The demagnetization factors are calculated incorrectly in Ref. 1, which alongwith other different parameters chosen in Ref. 5 will affect the energy dissipation comparison. While considering all these, Ref. 1's claims turn out to be untenable.

Moreover, Ref. 1 underestimates the resistance ratio r (actual expression is $r = (1 + \eta_1\eta_2 cos(\Theta))/(1 - \eta_1\eta_2)$ [Ref. 14]), does not mention the expressions for $E_{\phi 1}$ and $E_{\phi 2}$ in Eqs. (5) and (6) in the main Letter, compares with the spin-transfer-torque switching without considering scaling issue or using giant spin-Hall effect based switching, does not consider another $0.5CV^2$ energy dissipation during the *removal* of stress, and the *direction* of angle ζ is not consistent with the expressions in Eq. (1). Also, Ref. 1 states incorrectly that it needs to withdraw stress at the precise juncture $\theta = 90^\circ$ in Ref. 10 to switch magnetization completely by 180°. However, there is tolerance around $\theta = 90^\circ$, as described in Ref. 10. Such 180° switching (unlike the *incomplete* switching in Ref. 1) is claimed to be energy-efficient.[15,16]

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Comment on "Acoustically assisted spin-transfer-torque switching of nanomagnets: An energy-efficient hybrid writing scheme for non-volatile memory" [Appl. Phys. Lett. 103, 232401 (2013)]

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Ref. 1 claimed an energy-efficient way to write in spin-transfer-torque random access memory (STTRAM) using strain in piezoelectric-magnetostrictive heterostructures. Here, we show that the claim of energy-efficiency is incorrect while comparing to both traditional transistors and STTRAMs. Also the energy dissipation calculation due to *global* surface acoustic wave (SAW) is missing a crucial point that will invalidate the claim of energy-efficiency.

First, Ref. 1 follows the idea by Roy presented in the Ref. 2 (was not published due to the issues described here) with the addition of SAW and follows the formulation from Refs. 3 and 4. The basic idea was to switch the magnetization by STT along the desired direction when magnetization comes at the hard-plane ($\theta = 90°$, Fig. 1) upon application of stress.[2] However, thermal fluctuations creates an wide distribution for the time-delay when magnetization reaches at $\theta = 90°$.[5] This is why STT current needs be kept active for almost half of the duration of switching.[1] Ref. 5 proposed an attractive way to work with only stress by using a sensing element (spin-valve/MTJ) to detect when θ reaches *around* 90° (not at precise juncture as stated by Ref. 1).[5]

Figure 3 in Ref. 1 shows that the energy dissipation with a stress of 6.1 MPa is 5×10^9 kT at room-temperature (300 K), which is ∼20 pJ. This is 4-5 orders of magnitude higher than that of traditional transistors and therefore untenable for building nanoelectronics.[6,7]

Also, Fig. 3 in Ref. 1 shows the energy dissipation when no stress is present (only switching in STTRAM), which is $\sim 40 \times 10^9$ kT = 160 pJ. Note that Ref. 1 has considered the material Terfenol-D as free layer in STT switching to calculate the energy dissipation. However, the material that is commonly used for the free layer is CoFeB,[8–11] which has Gilbert damping parameter α an order lower[8,9] than Terfenol-D (α of Terfenol-D is 0.1 used by Ref. 1). The critical current of switching is proportional to damping parameter[8,9] and the energy dissipation is proportional to the square of the switching current. Therefore, Ref. 1 calculated *incorrectly* the switching current an order higher (23 mA) and energy dissipation about two orders higher (∼160 pJ) for STT switching (Ref. 8 *correctly* determined switching current ∼1 mA and energy dissipation ∼1 pJ experimentally).

Clearly, the comparison with STT switching performed in Ref. 1 is *incorrect* and actually the energy dissipation in STT switching is 12.5 times lower (in stead of 8 times higher as *incorrectly* claimed by Ref. 1) than the hybrid scheme proposed in Ref. 1. Note that CoFeB cannot be used as the magnetostrictive nanomagnet instead of Terfenol-D since CoFeB has 30 times lower magnetostriction coefficient than that of Terfenol-D requiring 30 times higher stress (and concomitant higher voltage) to generate the same stress anisotropy subjected to maximum strain allowed in the linear regime of stress-strain relation.

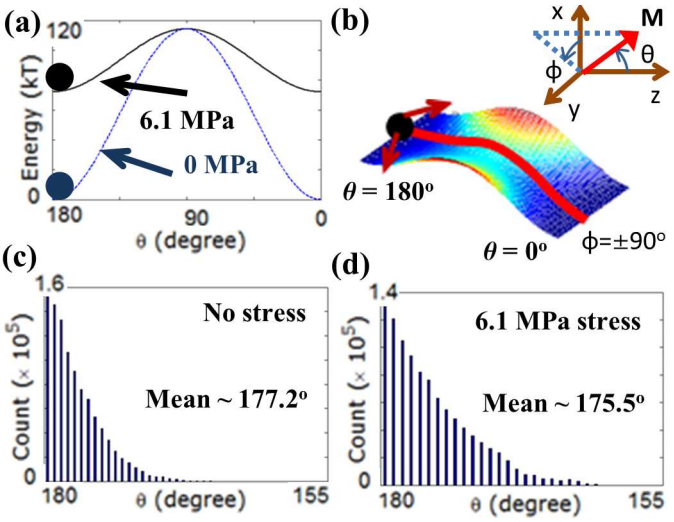

FIG. 1. (a) Potential landscapes of the nanomagnet with no stress and 6.1 MPa stress. (b) Three-dimensional potential landscape showing the deflection of magnetization out of magnet's plane (y-z plane, $\phi = \pm 90°$). (c) Room-temperature (300 K) thermal distribution of θ when no stress is active. (d) Room-temperature (300 K) thermal distribution of θ when 6.1 MPa stress is applied.

Also, the energy dissipation calculated due to SAW is missing a crucial point that will make the energy dissipation exceedingly high. Ref. 1 says that "SAW is "global" and affects every memory cell." This is represented in Fig. 1(a) that with the application of 6.1 MPa stress the barrier height decreases but it is not sufficient enough to make the potential landscape monostable and cause switching. However, when stress is applied the magnetization *does* rotate. The distribution in Fig. 1(d) upon application of stress is wider than the distribution in Fig. 1(c) when no stress is active. Therefore, the energy dissipation upon application of stress and removal of stress *must be calculated*, which is *missed* by Ref. 1. This energy dissipation turns out to be ∼40 kT for one

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cell. Considering just 1 MB memory, clearly such strategy would dissipate an energy which is quite worse than that of transistors.[6,7]

Fig. 1(b) depicts that magnetization may deflect out of magnet's plane when stress is applied. The torque due to stress acts in the out-of-plane ($\hat{\mathbf{e}}_\phi$ in Fig. 1(b)) direction as

$$\mathbf{T_{E,stress}} = -\hat{\mathbf{e}}_\mathbf{r} \times \nabla E_{stress} = -(3/2)\,\lambda_s \sigma \Omega sin(2\theta)\,\hat{\mathbf{e}}_\phi,$$

where $E_{stress} = -(3/2)\,\lambda_s \sigma \Omega cos^2\theta$ is the potential energy due to stress, $(3/2)\lambda_s$ is the magnetostrictive coefficient, σ is the stress, Ω is nanomagnet's volume. Therefore *magnetization rotates out-of-plane* even if the demagnetization factor in the out-of-plane direction is high ($\sim$10 times compared to the in-plane directions based on the chosen dimensions). This out-of-plane excursion has important ramification to increase switching speed,[3,5,12,13] which cannot be conceived if magnetization is *assumed* to reside always on magnet's plane as Ref. 14 did. This out-of-plane excursion depicted in the Fig. 1(b) is considered for the calculation of energy dissipation upon application of stress.

Note that the energy barrier height calculated in Ref. 1 is underestimated by $\sim$33% using the *assumption* of $a/b \sim 1$ (while a/b=110 nm/90 nm). In Ref. 1, the SAW frequency is 100 MHz and the lateral area of the devices are high (110×90 nm^2), which are clearly inferior to traditional transistors.[6,7] Refs. 15 and 16 are even more higher area consuming due to using lateral piezoelectric pads and also switching delay is high by about an order due to "toggle" switching.[15]

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Comment on "Bennett clocking of nanomagnetic logic using multiferroic single-domain nanomagnets" [Appl. Phys. Lett. 97, 173105 (2010)]

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In Ref. 1, Atulasimha and Bandyapadyay claimed Bennett clocking of nanomagnetic logic using 2-phase multiferroic composites. Here, we show that the analysis performed therein and the comparison with spin-transfer-torque (STT) switching of nanomagnets are incorrect and put it under perspective.

The basic *assumption* in Ref. 1 was that magnetization resides always on magnet's plane (y-z plane in Fig. 1), which is *not* correct. The torque due to stress acts in the out-of-plane ($\hat{\mathbf{e}}_\phi$ in Fig. 1) direction as

$$\mathbf{T_{E,stress}} = -\hat{\mathbf{e}}_\mathbf{r} \times \nabla E_{stress} = -(3/2)\,\lambda_s \sigma sin(2\theta)\,\hat{\mathbf{e}}_\phi,$$

where $E_{stress} = -(3/2)\,\lambda_s \sigma cos^2\theta$ is the potential energy due to stress per unit volume, $(3/2)\lambda_s$ is the magnetostrictive coefficient, and σ is the stress. Therefore *magnetization rotates out-of-plane* even if the demagnetization factor in the out-of-plane direction is high (about 8 times compared to the in-plane directions based on the chosen dimensions). This has a huge consequence at a finite temperature analysis.

If we calculate the switching delay of magnetization according to Ref. 1, it will come out ∼1000 ns, which is clearly untenable for building nanoelectronics.[2,3] While comparing with spin-transfer-torque (STT) switching mechanism, if one compares an usual performance metric i.e., switching delay-energy, clearly Ref. 1 performs inferior to STT switching. Also consider the issue that 1 hour of execution would take 100 hours or more using the operation presented in Ref. 1. If charge based transistors were to operate *slow*, the energy dissipation would not have been an issue.[2–4] There is also an issue on consuming more area[1] than that of STT or charge-base transistors and this will force us to use 100 computers instead of one for the same functionality.[2,3] The energy barrier height calculated in Ref. 1 is underestimated by ∼20% using the *assumption* of $a/b \sim 1$ (while a/b=105 nm/95 nm), and that higher barrier would require a concomitant amount of higher voltage (Ref. 1 follows the calculations from Ref. 5).

Recently, Ref. 6 performed a critical study on Bennett clocking in the presence of room-temperature thermal fluctuations with *correctly* taking into account the out-of-plane excursion of magnetization. Fig. 1 depicts the basic reasoning that magnetization gets deflected out-of-plane and thermal fluctuations create wide distributions during magnetization traversal. We can use a sensing

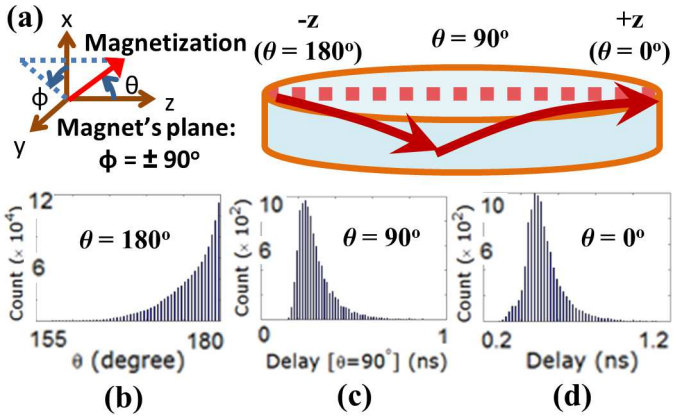

FIG. 1. Switching of magnetization at room-temperature.

element to detect when θ reaches around 90°, so that we can ramp down the stress thereafter.[7] There is tolerance however, i.e., θ does not need to be exactly 90°,[7] unlike stated in Ref. 8. The sensing element can be implemented by measuring the magnetoresistance in a spin-valve or magnetic tunnel junction (MTJ), which needs to be used anyway to read the magnetization state and it dissipates much less energy than for *write* operation.[7] We know the magnetoresistance of the MTJ when magnetization resides at $\theta = 90°$ (x-y plane) and comparing this known signal with the sensed signal of the MTJ, the stress can be ramped down.[7] Such comparator can be implemented with these energy-efficient multiferroic devices, i.e., charge-based transistors do not need to be utilized. It generally requires additional circuitry in conjunction with the basic device itself, without changing the order of dissipation with the respective devices.[4,9,10] Note that the "toggle" switch proposed in Ref. 8 [as stated "a write cycle must be preceded by a read cycle to determine the stored bit"] would require the very same sensing procedure using spin-valve or MTJ for reading the known bit, storing it, and then using it for comparison. Apart from that, Refs. 8 and 11 are highly area consuming due to using lateral piezoelectric pads and also switching delay is high by about an order.[8]

Ref. 12 predicted the demise of Bennett clocking mechanism in the presence of thermal fluctuations saying "This could render nanomagnetic logic schemes that rely on dipole coupling to perform Boolean logic operations." However, Ref. 6 analyzes the key issue and such dynamic release of stress is the *basic requirement* to function and to achieve successful switching.[7,10,13,14] No pulse-shaping methodology[15] can get us far in achieving a low-error

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probability alongwith a low switching delay for technological applications. The out-of-plane excursion of magnetization makes the magnetization switching *fast* in sub-nanosecond delay[7,10,13,14] Also, this dynamic release of stress can work with finite ramp-rate of stress,[7] consideration of which would make Ref. 8 *unreliable*, as stress is unreasonably *assumed* to be *instantaneous*.

Rather than using Bennett clocking for building logic, a more intriguing way to construct logic would be to use a single device with a read-unit (MTJ) as a switch (similar to a transistor acting as a switch) or even universal logic gates (NAND/NOR) can be built with well-established way of using multiple contacts on the device to add up the strains generated in piezoelectric, and a *Set* input to preset the non-volatile magnetization state and facilitate concatenation.[16]

Using spin-torque to switch magnetization in multiferroic composites[17] would dissipate ∼20 pJ (Ref. 18), which is 4-5 orders of magnitude higher than that of traditional transistors[2,3] and there is also proposal of *incomplete* switching of magnetization.[11] Recently, Ref. 19 showed that interface magnetoelectric effect and exchange coupling can maintain the direction of switching unlike *toggle* switching, without any requirement of any sensing circuitry,[7,8] alongwith promising performance metrics for area, delay, and energy dissipation. This can be utilized for logic design.[6,16] Experimental efforts in this field are evolving and the theoretical concepts described here would play an important role in possibly devising the switching methodology and nanomagnetic logic.

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